WHAT IS CLAIMED IS:

1. A multiprocessor system comprising:

two or more processor elements whose performances are to be executed by a common program;

a control section for switching such plural processor elements one from another for execution by said common program; and

a storing section, responsive to each switching of said processor elements by said control section, for storing handover information relating to the common program which information is to be handed over from said one processor element to said another processor element.

2. A multiprocessor system according to claim 1, wherein, with the switching of said processor elements, said control section stores said handover information from said one processor element into said storing section and then stops the performance of said one processor element and, at the same time, starts the performance of said another processor element using said handover information stored in said storing section.

3. A multiprocessor system according to claim 1, wherein, if a performance requested to be executed for one of said plural processor elements is to be

made by another processor element, said last-named one processor element outputs a switching request signal to said control section for switching said processor elements from said last-named one processor element to the last-named another processor element.

4. A multiprocessor system according to claim 2, wherein, if a performance requested to be executed for one processor element is to be made by another processor element, the last-named one processor element outputs a switching request signal to said control section for switching said processor elements from said last-named one processor element to the last-named another processor element.

5. A multiprocessor system according to claim 3, wherein said switching request signal is a switching control interruption signal.

6. A multiprocessor system according to claim 4, wherein said switching request signal is a switching control interruption signal.

7. A multiprocessor system according to claim 1, wherein, upon receipt of a signal from outside said system, said control section outputs an interruption signal to the last-named another processor element

to stop the performance thereof.

8. A multiprocessor system according to claim 2, wherein, upon receipt of a signal from outside said system, said control section outputs an interruption signal to said another processor element to stop the performance thereof.

9. A multiprocessor system according to claim 3, wherein, upon receipt of a signal from outside said system, said control section outputs an interruption signal to said last-named another processor element to stop the performance thereof.

10. A multiprocessor system according to claim 4, wherein, upon receipt of a signal from outside said system, said control section outputs an interruption signal to said last-named another processor element to stop the performance thereof.

11. A multiprocessor system according to claim 5, wherein, upon receipt of a signal from outside said system, said control section outputs an interruption signal to said last-named processor element to stop the performance thereof.

12. A multiprocessor system according to claim 6,

wherein, upon receipt of a signal from, said control section outputs an interruption signal to said last-named processor element to stop the performance thereof.

13. A multiprocessor system according to claim 1, wherein said control section has a table for indicating, for designation of one at a time from said plural processor elements, a permitted-to-perform processor element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

14. A multiprocessor system according to claim 2, wherein said control section has a table for indicating, for designation of one at a time among said plural processor elements, a permitted-to perform processor element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

15. A multiprocessor system according to claim 3, wherein said control section has a table for indicating, for designation of one at a time among said plural processor elements, a permitted-to-perform processor

element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

16. A multiprocessor system according to claim 4, wherein said control section has a table for indicating, for designation of one at a time among said plural processor elements, a permitted-to-perform processor element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

17. A multiprocessor system according to claim 5, wherein said control section has a table for indicating, for designation of one at a time among said plural processor elements, a permitted-to-perform processor element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

18. A multiprocessor system according to claim 6, wherein said control section has a table for indicating, for designation of one at a time among said plural processor elements, a permitted-to-perform processor

element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

19. A multiprocessor system according to claim 7, wherein said control section has a table for indicating, for designation of one at a time among said plural processor elements, a permitted-to-perform processor element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

20. A multiprocessor system according to claim 8, wherein said control section has a table for indicating, for designation of one at a time among said plural processor elements, a permitted-to-perform processor element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

21. A multiprocessor system according to claim 9, wherein said control section has a table for indicating, for designation of one at a time among said plural

processor elements, a permitted-to-perform processor element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

22. A multiprocessor system according to claim 10, wherein said control section has a table for indicating, for designation of one at a time among said plural processor elements, a permitted-to-perform processor element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

23. A multiprocessor system according to claim 11, wherein said control section has a table for indicating, for designation of one at a time among said plural processor elements, a permitted-to-perform processor element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

24. A multiprocessor system according to claim 12, wherein said control section has a table for indicating, for designation of one at a time among said plural

processor elements, a permitted-to-perform processor element, which is allowed to perform processing, and controls the switching of said processor elements so as to designate said permitted-to-perform processor element based on said table.

25. A multiprocessor system according to claim 13, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

26. A multiprocessor system according to claim 14, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

27. A multiprocessor system according to claim 15, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said last-named another processor element, and outputs an

interruption signal to said permitted-to-perform processor element to stop the performance thereof.

28. A multiprocessor system according to claim 16, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said last-named another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

29. A multiprocessor system according to claim 17, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said last-named another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

30. A multiprocessor system according to claim 18, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said last-named another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

31. A multiprocessor system according to claim 19, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said last-named another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

32. A multiprocessor system according to claim 20, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said last-named another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

33. A multiprocessor system according to claim 21, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said last-named another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

34. A multiprocessor system according to claim 22, wherein, with consulting said table, said control section selects said permitted-to-perform processor

element, which is indicated by said table, as said last-named another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

35. A multiprocessor system according to claim 23, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said last-named another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

36. A multiprocessor system according to claim 24, wherein, with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said last-named another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof.

37. A multiprocessor system according to claim 1, wherein said control section actuates one of said plural processor elements with precedence over the remaining processor elements, and actuates one of said remaining processor elements in place of the second-to-last-named one processor element as demand

arises.

38. A multiprocessor system according to claim 1, wherein said plural processor elements are different in function from one another.

39. A multiprocessor system according to claim 38, wherein, upon receipt of a signal from outside said system, said control section selects, from said plural processor elements, one processor element to handle the last-named signal, and actuates the selected one processor element.

40. A multiprocessor system according to claim 38, wherein at least one of said plural processor element is an MPU (Micro Processing Unit) and the remainder is a DSP (Digital Signal Processor), or vice versa.

41. A multiprocessor system according to claim 39, wherein at least one of said plural processor element is an MPU (Micro Processing Unit) and the remainder is a DSP (Digital Signal Processor), and vice versa.

42. A multiprocessor system according to claim 1, further comprising an invalidating section for invalidating the switching function of said control section to thereby actuate at least two or more of

said plural processor elements simultaneously.

43. A multiprocessor system according to claim 1, wherein said handover information to be stored in said storing section includes at least one selected from the group consisting of a value of a program counter, an argument of a function, a return value of a function, and content of a stack pointer.

44. A multiprocessor control method for switching two or more processor elements of a multiprocessor system, whose performances are to be executed by a common program, said control method comprising the steps of:

(a) in response to each switching of said processor elements, storing handover information relating to the common program, which information is to be handed over from said one processor element to said another processor element, into a storing section of said multiprocessor system; and

(b)after said handover information has been stored into the storing section, stopping the performance of said one processor element and starting said another processor element using said handover information stored in the storing section.

45. A computer-readable recording medium in which a multiprocessor control program for switching two or

more processor elements of a multiprocessor system, whose performances are to be executed by a common program, wherein said multiprocessor control program instructs a computer at the system to execute the steps of:

(a) in response to each switching of said processor elements, storing handover information relating to the common program, which is to be handed over from said one processor element to said another processor element into a storing section of said multiprocessor system; and

(b) after said handover information has been stored into the storing section, stopping the performance of said one processor element and stopping the performance of said another processor element using said handover information stored in said storing section.